REMARKS

I. Introduction

Applicants express appreciation for Examiner Huisman's courtesy and professionalism in conducting a telephonic interview on October 7, 2004.

In response to the Office Action mailed July 12, 2004, Applicants have amended the Title of the Invention to more accurately describe the present invention. Applicants have amended claims 1 and 5 so as to further clarify the claimed subject matter. Applicants have also added new claim 21. Support for these amendments can be found, for example, in Figs. 1 and 2, and their corresponding section of the specification. No new matter has been added.

For the reasons set forth below, Applicants respectfully submit that all pending claims are patentable over the cited prior art references.

II. The Rejection Of The Claims Under 35 U.S.C. § 102

Claims 1-3, 5, 7-10 and 12-15 are rejected under 35 U.S.C. § 102(b) as being anticipated by USP No. 5,506,976 to Jaggar. Applicants respectfully traverse this rejection for at least the following reasons.

Claim 1, as amended, recites in-part to a processor comprising detecting means for detecting that the instruction to be executed by the instruction executing means is a last instruction of a process before branching, wherein the detecting means detects by comparing information corresponding to the instruction to be executed by the executing means and a predetermined information in accordance with the process in execution one by one. Claim 5 recites in-part a processor, wherein the detecting means detects the last instruction based on judgment whether

information stored in correspondence with information indicating a content of an instruction to be executed by the instruction executing means in the storing means indicates the last instruction.

In the pending rejection, it is asserted that the program counter 10, reach value register 16, comparator 14 and branch cache 4 correspond to the claimed detecting means. Turning to the cited prior art, Jaggar discloses that the comparator 14 compares the lowermost eight bits between the program counter value PC and the reach value R in the reach value latch 16, which is a *preliminary comparison* before the program counter value PC is compared with the cache tags within the branch cache 4 (see, col. 6, line 49-col. 7, line 19). More specifically, the enable signal is asserted ON by the comparator 14 when the comparator 14 determines that the reach value R currently stored within the reach value latch 16 matches the lower order bits of the program counter value PC stored within the program counter register 10. If the instruction addresses are 16-bit addresses, then storage capacity within the branch cache 4 can be saved by only requiring the reach value R to be an eight-bit word. In this manner, the reach value R is compared with the lowermost eight bits of the program counter value PC. The branch cache 4 then compares the value of the full instruction address in parallel with all of the cache tags.

However, as discussed during the interview, the detecting means of the present invention does not require such a *preliminary comparison*. Indeed, in accordance with one embodiment of the present invention, the detecting means compares the addresses, such as fetch address and end address, one by one. For example, the comparator 136 compares the end addresses stored in the end address storing parts 121 to 123 one by one. As such, in contrast to the conclusion set forth in the pending rejection, the detecting means of the present invention is fundamentally different from the alleged detecting means comprising the comparator 13 and the branch cache 4 of Jaggar.

Thus, at a minimum, Jaggar does not disclose or suggest detecting means for detecting that the instruction to be executed by the instruction executing means is a last instruction of a process before branching, wherein the detecting means detects by comparing information corresponding to the instruction to be executed by the executing means and a predetermined information in accordance with the process in execution one by one, as recited by amended claim 1, or that the detecting means detects the last instruction based on judgment whether information stored in correspondence with information indicating a content of an instruction to be executed by the instruction executing means in the storing means indicates the last instruction, as recited by amended claim 5.

Furthermore, Jaggar requires that the branch instruction detector 22 detects the last instruction before branching by detecting the branch instruction in order to automatically set the cache data in each cache line 12 (see, Fig. 1 and col. 7, lines 39-46). In contrast, the present invention does not require such a branch instruction detector for detecting the last instruction before branching any instruction.

Moreover, Jaggar discloses that the processor has a branch cache 4 so as to branch the process immediately after a tag is hit. However, the program counter value PC must be compared in parallel with the cache tag values of each of the cache lines 12, and thus the processor of Jaggar requires a large hardware scale and much power consumption. Indeed, the comparator 14 of Jaggar compares two values preliminarily so as to reduce the power consumption. As such, even when the values match in the preliminary comparison and that the branch cache 4 compares each value in parallel with all of the cache tags, significant power consumption is still required. Thus, the branch instruction detector 22 causes an increase of the hardware scale and the power consumption.

In contrast, in accordance with one embodiment of the present invention, the detecting means is different from the comparator 13 and the branch cache 4 of Jaggar. Specifically, the detecting means of the present invention detects whether the instruction to be executed by the instruction executing means is a last instruction of a process before branching. As such, the processor of the present invention requires very small hardware scale, minimal power consumption, and relatively short programs having several steps that can be executed repeatedly at high speed.

Thus, at a minimum, Jagger does not disclose or suggest that the detecting means for detecting that the instruction to be executed by the instruction executing means is a last instruction of a process before branching, as recited by amended claims 1 and 5.

As anticipation under 35 U.S.C. § 102 requires that each element of the claim in issue be found, either expressly described or under principles of inherency, in a single prior art reference, *Kalman v. Kimberly-Clark Corp., 713 F.2d 760, 218 USPQ 781 (Fed. Cir. 1983)*, and at a minimum, Jaggar fails to disclose the foregoing claim elements, it is clear that Jaggar does not anticipate claim 1, or 5, or any of the claims dependent thereon.

III. All Dependent Claims Are Allowable Because The Independent Claims From Which They Depend Are Allowable

Under Federal Circuit guidelines, a dependent claim is nonobvious if the independent claim upon which it depends is allowable because all the limitations of the independent claim are contained in the dependent claims, *Hartness International Inc. v. Simplimatic Engineering Co., 819 F.2d at 1100, 1108 (Fed. Cir. 1987)*. Accordingly, as claims 1 and 5 are patentable for the reasons set forth above, it is respectfully submitted that all claims dependent thereon are also in condition for allowance.

For all of the foregoing reasons, it is submitted that claims 2-4 and 6-20 are patentable over the cited prior art. Accordingly, it is respectfully requested that the rejections of claims 1-3, 5, 7-10 and 12-15 under 35 U.S.C. § 102, and claims 4, 6, 11 and 16-20 under 35 U.S.C. § 103 be withdrawn.

IV. Conclusion

Accordingly, it is urged that the application is in condition for allowance, an indication of which is respectfully solicited.

If there are any outstanding issues that might be resolved by an interview or an Examiner's amendment, the Examiner is requested to call Applicants' attorney at the telephone number shown below.

To the extent necessary, a petition for an extension of time under 37 C.F.R. § 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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